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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,981	07/18/2003	Christian May	P2001,0025	2995
24131	7590	10/04/2005	EXAMINER	
LERNER AND GREENBERG, PA P O BOX 2480 HOLLYWOOD, FL 33022-2480			PAN, DANIEL H	
			ART UNIT	PAPER NUMBER
			2183	
DATE MAILED: 10/04/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/622,981

Applicant(s)

MAY ET AL.

Examiner

Daniel Pan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 July 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 04/25/05, 07/18/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

1. Claims 1-17 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-5,9-12,14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamber (6,047,365) in view of Fitch et al. (5,056,060).
2. As to claims 1,12, 14,15, Chambers taught a microprocessor circuit, comprising:  
at least :
  - a) one control unit [300] [312][316] ;
  - b) one memory (see fig.1C [16] for overall structure, see fig.3 [306]) for free programming with at least one program having functions (see DRAM as system memory, it is free for programming because it is a system memory) , the memory connected to the control unit (see fig.3);
  - c) a stack [306] for buffer-storing data (see memory wave table sample page of 4k byte in col.5, lines 1-9) , the stack connected to the control unit;
  - d) a register bank having registers [308] , the register bank connected to said control unit; and
  - e) an auxiliary register storing a number of bits (see valid bit register ) , each of the

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bits being associated with one of said registers of the register bank (see register bank 308) and indicating whether a respective one of the registers contained valid bit (see col.5, lines 28-46), the auxiliary register [valid bit register 310] connected to at least one of the control unit, the register bank [308], and a stack [306].

3. Chamber did not specifically show his auxiliary register contained a value different from a logical "0" as claimed. However, Fitch taught a logical 1 for a valid determination (see col.15, lines 40-45, see the logical "1" as valid signal). It would have been obvious to one of ordinary skill in the art to use Fitch in Chambers for including a value different from logical "0" (i.e. logical "1") as claimed because the use of Fitch could provide the capability of Chamber to determine the validity of his register content based on the logic comparison, thereby minimizing the use of extra hardware overheads based on a single logical result, such as ("1" or "0"), and because although Chamber did not show how the logical determination was made, of ordinary skill in the art should be able to recognize Fitch's logical 1, which was different from logical "0", could be applicable for determine the valid bit of the register in order to provide logical comparison in Chamber. The examiner hold that the use of logical states, such as "0" or "1" should be well within the skill of ordinary in the art, and applicable in many applications. Fitch is used to show the logical value could be used for a valid determination, and since Chamber already taught the valid determination, and since no specific application has been reflected into he claim, it provided a suggestion to

combined in order to provide the single comparison logical result, and in doing so, provided a motivation.

4. \*As to claims 2,3, 4, Chamber also included further registers (see the greater and lesser number of registers in col.5, lines 40-47).

5. As to claim 5, Chamber's register was also in the same register bank (see fig.3[308]).

6. \*As to claims 9,10, Chamber also showed first and second areas (see the corresponding address space in fig.3).

7. As to claim 11, Chamber also divided in sub areas (see portions [308] memory bank in fig.3).

8. Claims 6,7, 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamber (6,047,365) in view of Fitch et al. (5,056,060) as applied to claims 1, 12 and further in view of Arnold et al. (4,558,176).

9. As to claims 6,7,8, neither Chamber nor Fitch specifically showed the inaccessible stack as claimed however, Arnold disclosed a control stack inaccessible by external modifications ( col.13, lines 28-44). It would have been obvious to one of ordinary skill in the art to use Arnold in Chamber for including the inaccessible stack as claimed because the use of Arnold could provide Chamber the ability to protect the content of his stack, and because Chamber taught a read only memory (see col.1, lines 16-32), which was not write accessible, and one of ordinary skill in the art should be

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able to recognize the applicability of either read, write or both permissions in a memory in order to protect the content of the register bank for a particular application, and for above reasons, provided a motivation.

10. Claims 13, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamber (6,047,365) in view of Fitch et al. (5,056,060) as applied to claim 12 and further in view of Wright et al. (4,802,218).

11. As to claims 13, neither Chamber nor Fitch specifically show the permission of the data in the register bank as claimed. However, Wright disclosed a system for permitting readings of a memory section (see the locked memory section in Col.16, lines 60-65). It would have been obvious to one of ordinary skill in the art to use Wright in Chamber for including the reading permission as claimed because Chamber taught a read only memory (see col.1, lines 16-32), which was not write accessible, and one of ordinary skill in the art should be able to recognize the applicability of either read, write or both permissions in a memory in order to lock the data of the register bank for a specific application, and for above reasons, provided a motivation.

12. As to claims 16,17, Wright also stored data in memory after a first function (see the record updated in col.17, lines 1-14).

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Holtery et al. (5,293,424) is cited for the teaching of access control memory (see fig.2, col.5, lines 27-68).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**21 Century Strategic Plan**

DANIEL H. PAN  
PRIMARY EXAMINER  
GROUP

